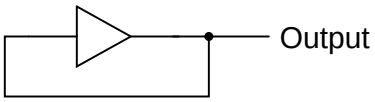

Introducing Sequential Logic: Latches

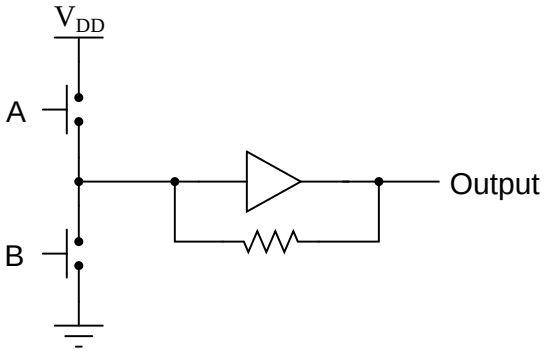
Questions

Question 1

What do you think this logic buffer gate will do, with the output signal "feeding back" to the input?



What do you think this buffer will do when each input switch is separately pressed?



Why does the second buffer circuit need a resistor in the feedback loop?

file 02896

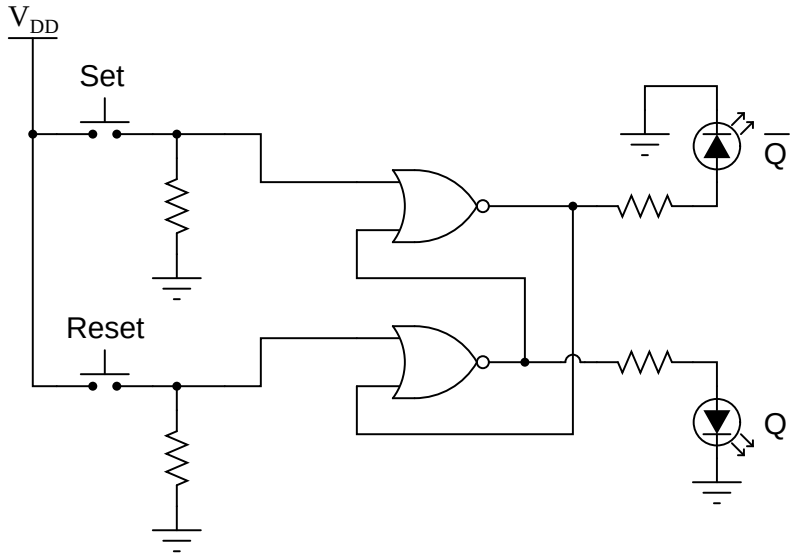
Question 2

When studying latch circuits, you will come across many references to *set* and *reset* logic states. Give a simple definition for each of these terms in the context of latch and flip-flop circuits.

file 02897

Question 3

The circuit shown here is called an *S-R latch*:



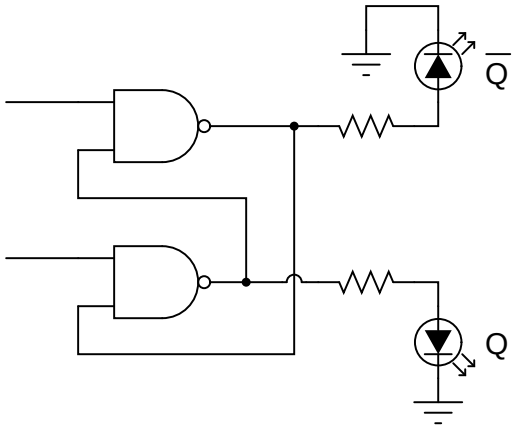
Complete the truth table for this latch circuit:

Set	Reset	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

file 01349

Question 4

The circuit shown here is called an *S-R latch*:



Identify which of the two input lines is the *Set*, and which is the *Reset*, and then write a truth table describing the function of this circuit.

file 01351

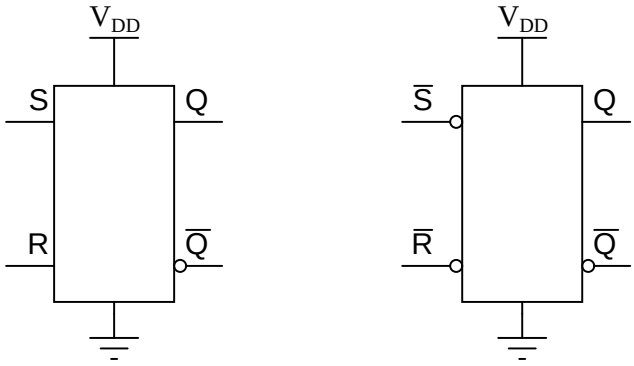
Question 5

Some digital circuits are considered to have *active-low* inputs, while others have *active-high* inputs. Explain what each of these terms means, and how we might identify which type of input(s) a digital circuit has.

file 02898

Question 6

Latch circuits are often drawn as complete units in their own block symbols, rather than as a collection of individual gates:



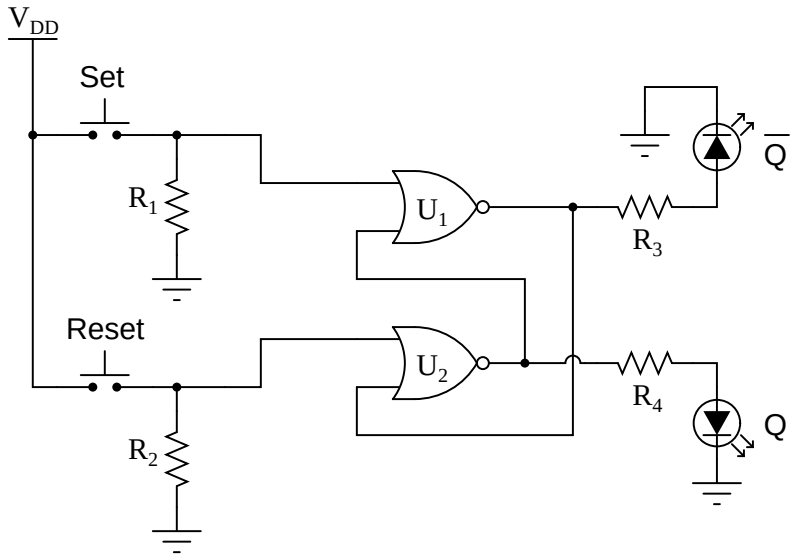
This simplifies schematic drawings where latches are used, much as the use of gate symbolism (as opposed to drawing individual transistors and resistors) simplifies the diagrams of more elementary digital circuits.

From the block symbols shown in this question, is there any way to determine which of the S-R latches is built with NOR gates, and which one is built with NAND gates?

file 01352

Question 7

Identify at least one component fault that would cause the "$\overline{Q}$" LED to always remain off, no matter what was done with the input switches.

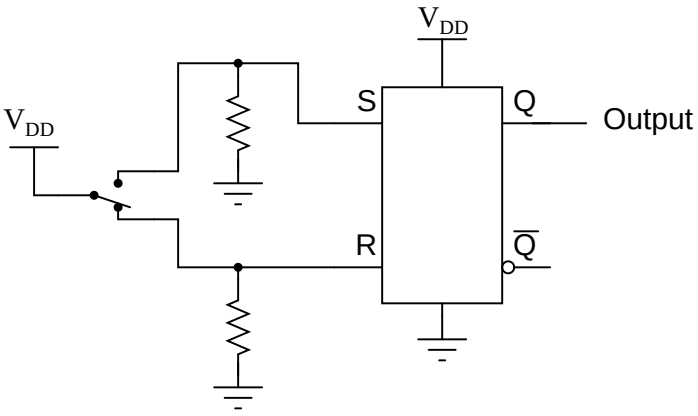


For each of your proposed faults, explain *why* it will cause the described problem.

file 03892

Question 8

One practical application of S-R latch circuits is *switch debouncing*. Explain what "bounce" refers to in mechanical switches, and also explain how this circuit eliminates it:

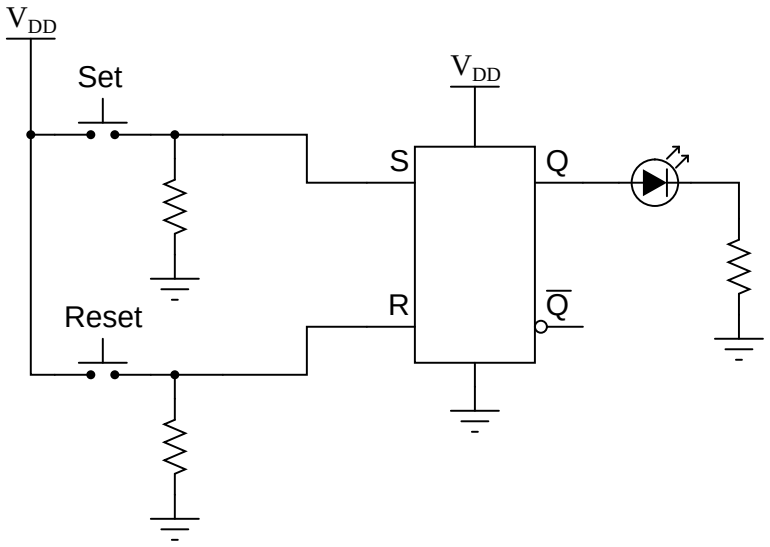


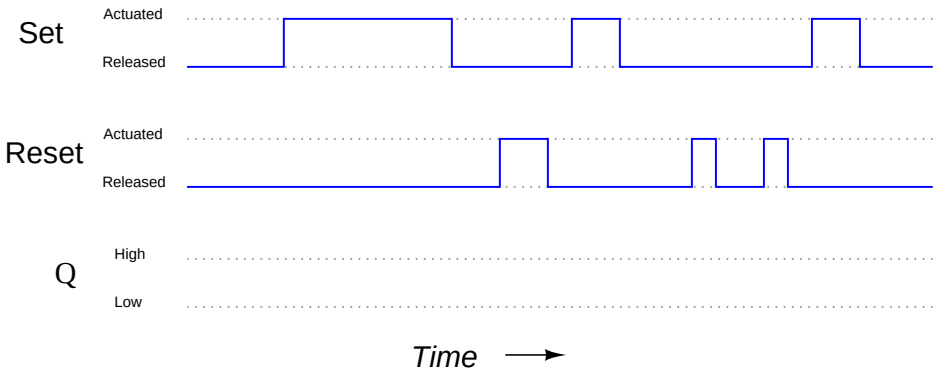
Also, show where an oscilloscope could be connected to display any switch "bounce," and explain how the oscilloscope would have to be configured to capture this transient event.

file 01353

Question 9

Complete the timing diagram, showing the state of the Q output over time as the Set and Reset switches are actuated. Assume that Q begins in the low state on power-up:

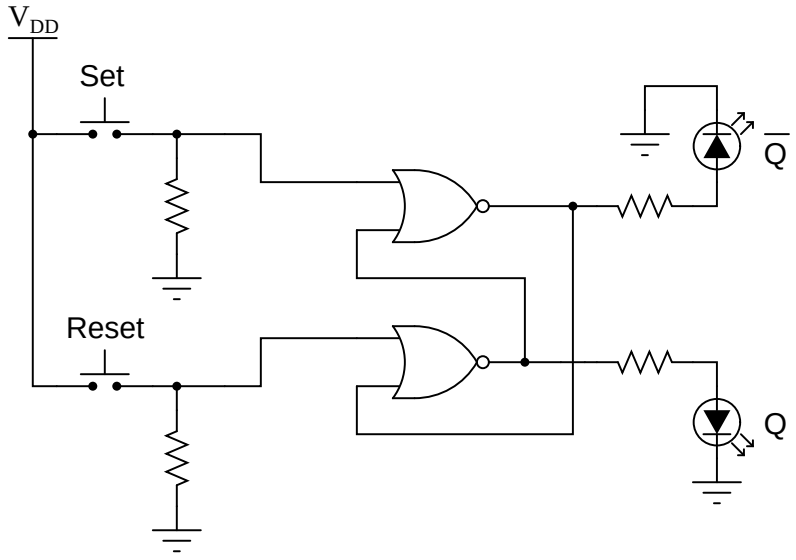




file 02899

Question 10

A student builds this simple S-R latch for their lab experiment:



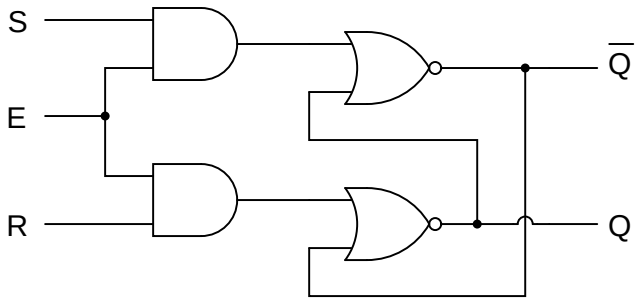
When the student powers up this circuit, she notices something strange. Sometimes the latch powers up in the *set* state (Q high and $\overline{Q}$ low), and other times it powers up in the *reset* state (Q low and $\overline{Q}$ high). The power-up state of their circuit seems to be unpredictable.

What state *should* their circuit power up in? Did the student make an error building the latch circuit?

file 01378

Question 11

The circuit shown here is a *gated* S-R latch. Write the truth table for this latch circuit, and explain the function of the "Enable" (E) input:

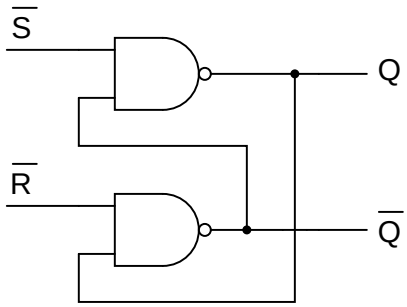


E	S	R	Q	$\overline{Q}$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

file 01354

Question 12

Here is an S-R latch circuit, built from NAND gates:

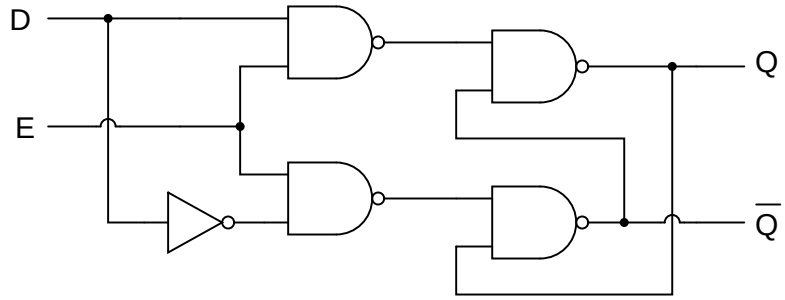


Add two more NAND gates to this circuit, converting it into a *gated* S-R latch, with an Enable (E) input, and write the truth table for the new circuit.

file 01355

Question 13

A variation on the gated S-R latch circuit is something called the *D-latch*:



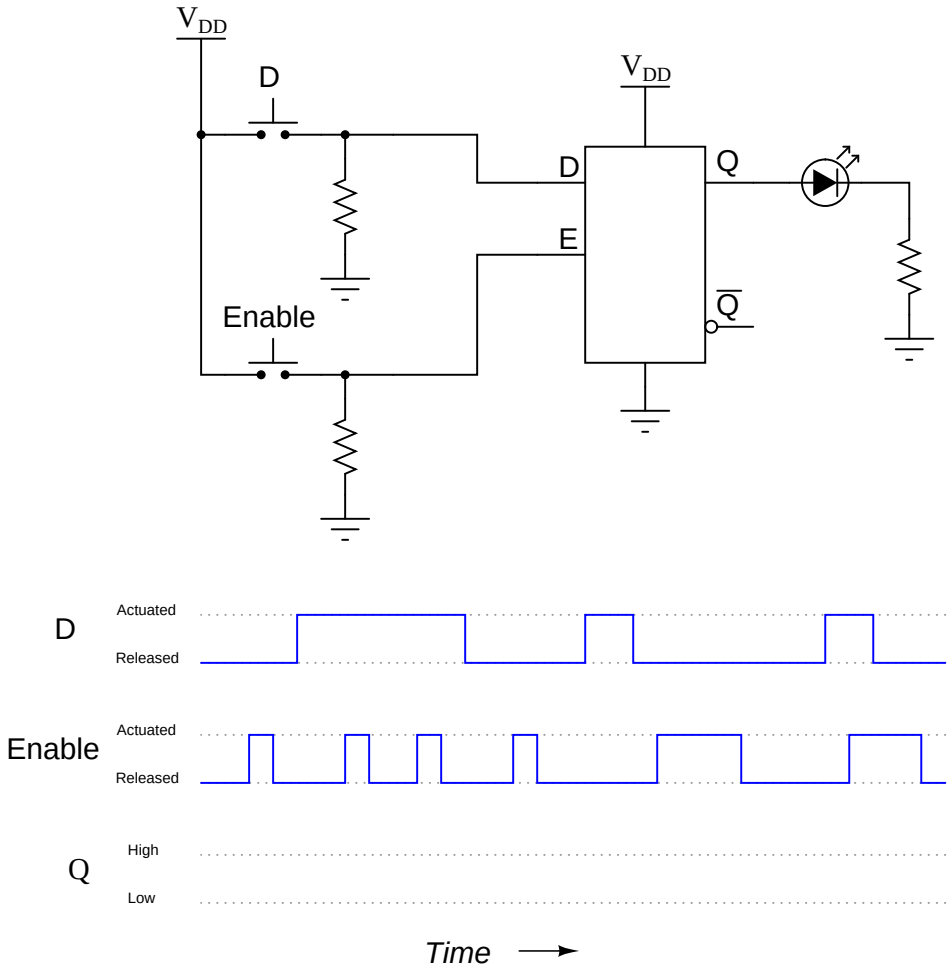
E	D	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

Complete the truth table for this D latch circuit, and identify which rows in the truth table represent the *set*, *reset*, and *latch* states, respectively.

file 01357

Question 14

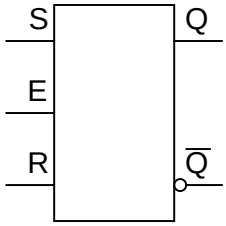
Complete the timing diagram, showing the state of the Q output over time as the input switches are actuated. Assume that Q begins in the low state on power-up:

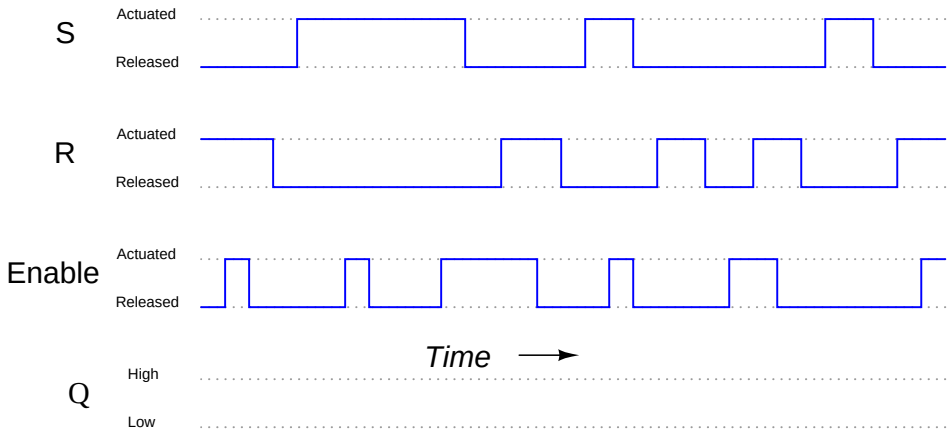


file 02901

Question 15

Complete the timing diagram, showing the state of the Q output over time as the input switches are actuated. Assume that Q begins in the low state on power-up:

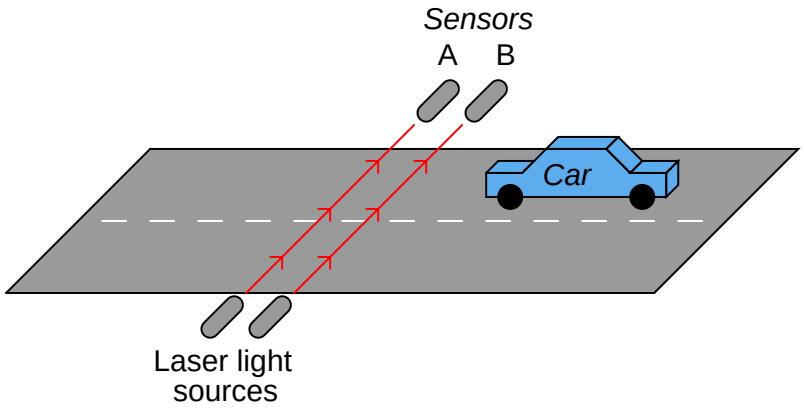




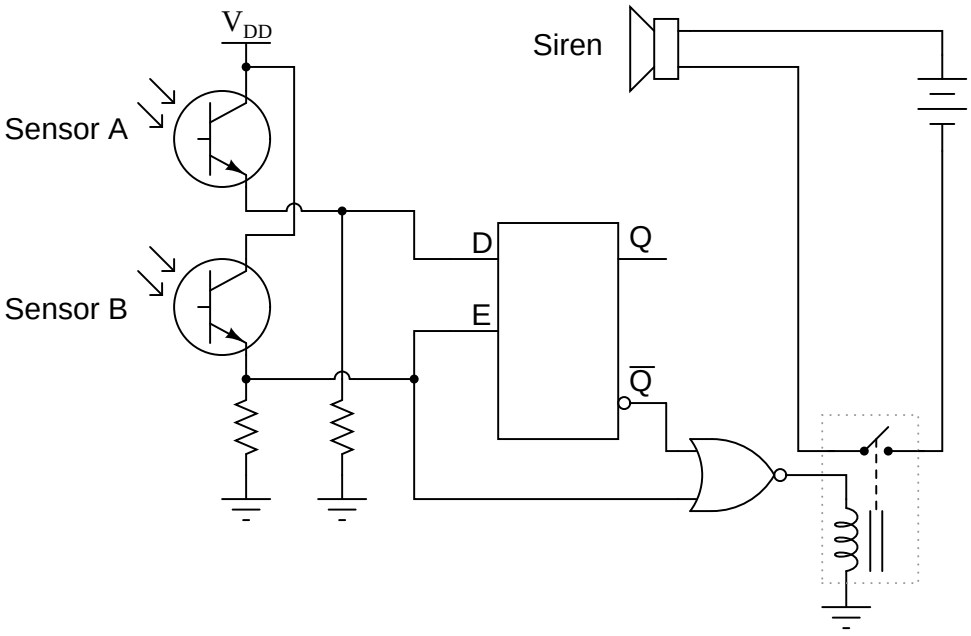
file 02913

Question 16

This one-way street is equipped with an alarm to signal drivers going the wrong way. The sensors work by light beams being broken when an automobile passes between them. The distance between the sensors is less than the length of a normal car, which means as a car passes by, first one beam is broken, then both beams become broken, then only the last beam is broken, then neither beam is broken. The sensors are phototransistors sensitive only to the narrow spectrum of light emitted by the laser light sources, so that ambient sunlight will not "fool" them:



Both sensors connect to inputs on a D-type latch, which is then connected to some other circuitry to sound an alarm when a car goes down the road the wrong way:



The first question is this: which way is the *correct* way to drive down this street? From left to right, or from right to left (as shown in the illustration)?

The second question is, how will the system respond if sensor A's laser light source fails? What will happen if sensor B's laser light source fails?

file 01361

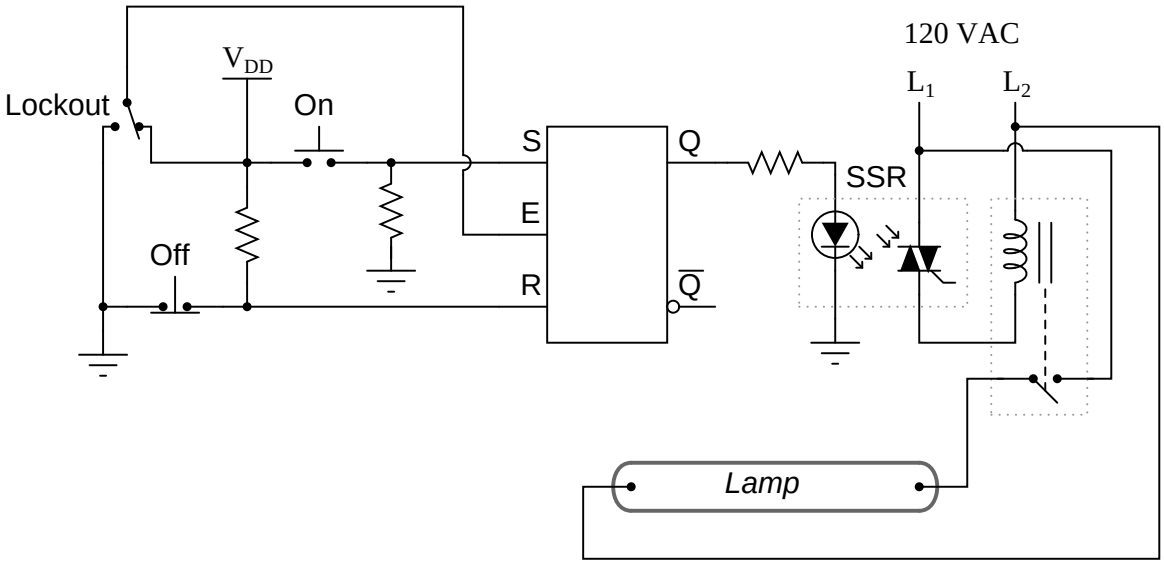
Question 17

Latch circuits such as the S-R latch and the D latch are often referred to as *transparent* digital devices. Explain what this term means, and why latches are classified as such.

file 03984

Question 18

Here, a gated S-R latch is being used to control the electric power to a powerful ultraviolet lamp, used for sterilization of instruments in a laboratory environment:



Based on your knowledge of how gated S-R latches function, what is the purpose of the "Lockout" switch? Also, explain how the CMOS latch is able to exert control over the high-power lamp (i.e. explain the operation of the interposing devices between the latch and the lamp).

Now, suppose the lab personnel want to add a feature to the ultraviolet sterilization chamber: an electric solenoid door lock, so that personnel can open the door to the chamber only if the following conditions are met:

- Lamp is *off*
- "Lockout" switch is sending a "low" signal to the latch's Enable input

Modify this circuit so that it energizes the door lock solenoid, allowing access to the chamber, only if the above conditions are both true.

file 01356