DUBLIN CITY UNIVERSITY

SAMPLE EXAMINATION 2012/2013

MODULE:	EE223 Digital and Analogue Electronics
QUALIFICATION:	EE - BEng in Electronic Engineering ME - B.Eng. in Mechatronic Engineering DME - B.Eng. in Digital Media Engineering ICE - BEng Info and Communications Engineering AP – BSc in Applied Physics PHA – BSc in Physics with Astronomy PBM – BSc in Physics with Biomedical Sciences ECSAO - Study Abroad (Eng.& Comp.)
YEAR:	2
EXAMINERS:	Dr. Derek Molloy, Ext no. 5355 Prof. William Buchanan Prof. Sakir Sezer
TIME ALLOWED:	2 Hours
INSTRUCTIONS:	Please answer any 4 questions. All questions carry equal marks.

Requirements for this paper
Please mark (X) as appropriate

	Log Tables
X	***Graph Paper***

Please do not turn over this page until you are instructed to do so

The use of programmable or text storing calculators is expressly forbidden.

Please note that where a candidate answers more than the required number of questions, the examiner will mark all questions attempted and then select the highest scoring ones

QUESTION 1 **[TOTAL MARKS: 25]**

An industrial system has several sensors (A, B, C, D) to determine if a process is working correctly. A warning light should come on if:

- Sensors B and C are activated, but A and D are not activated.
- Sensors A and C are activated, but B and D are not activated.
- Sensors A, C and D are activated, but B is not activated.
- Sensors A, B and C are activated, but D is not activated.
- Sensors A, B, C and D are activated.

Question 1(a) **[4 Marks]**

Present a *truth table* for this system.

Question 1(b) **[7 Marks]**

Derive, using a *Karnaugh Map*, a minimal sum-of-products function for this system.

Question 1(c) **[3 Marks]**

Present a circuit, using only AND/OR/NOT gates, implementing the function derived in part (b). Assume that each gate can have any number of inputs.

Question 1(d) **[6 Marks]**

Using *De Morgan's Theorem(s)*, design a circuit, using only NAND gates, that will implement the function derived in part (b). Assume that each logic gate can have any number of inputs and that inverted inputs are available.

Question 1(e) **[5 Marks]**

Prove the following theorem of Boolean algebra: $A + \overline{A}B = A + B$

[End of Question 1]

QUESTION 2 **[TOTAL MARKS: 25]**

Question 2(a) **[6 marks]**

Using logic gates, design a circuit that adds two binary bits and a *carry in* (C_{in}) bit together, producing a *Sum* (Σ) and a *carry out* (C_{out}) output as illustrated in Figure 2.1. Does this figure describe a full adder or a half adder circuit?

[PTO…]

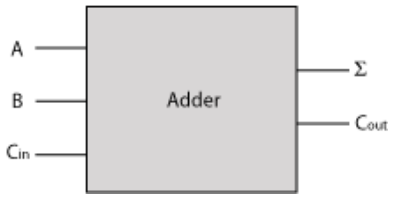

Figure 2.1 An Adder

Question 2(b) **[7 marks]**

In relation to place-weighted numeration systems, describe how many valid ciphers exist in the hexadecimal system, and the respective "weights" of each place in a hexadecimal number.

Also, perform the following conversions (show each step clearly):
- 35_{16} into decimal
- 34_{10} into hexadecimal
- 11100010_2 into hexadecimal
- 93_{16} into binary

Question 2(c) **[6 Marks]**

With the aid of a diagram, explain the operation of a full-wave bridge rectifier circuit with an alternating (AC) voltage input.

Question 2(d) **[6 marks]**

A full wave rectifier uses silicon diodes and has an input voltage as shown below in Figure 2.2.

i) What will the output waveform look like? (Take the turn-on voltage of a silicon diode to be 0.6V).
ii) Assuming fast enough switching, calculate the mean (DC) output voltage level.

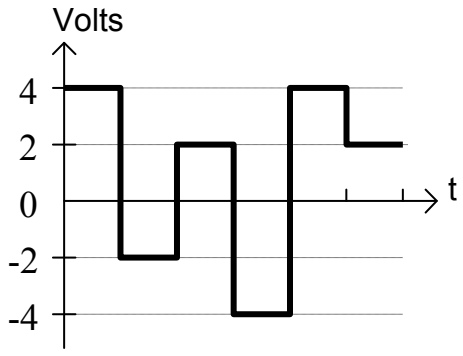

Figure 2.2 The input to a full-wave rectifier

[End of Question 2]

QUESTION 3 **[TOTAL MARKS: 25]**

Question 3(a) **[10 marks]**

Figure 3.1 illustrates a circuit that contains a D-type gated latch. There is a string of NOT gates before an AND gate – why would we use such a circuit? Given the inputs described in the graph below, describe the input E and then describe the outputs Q and /Q.

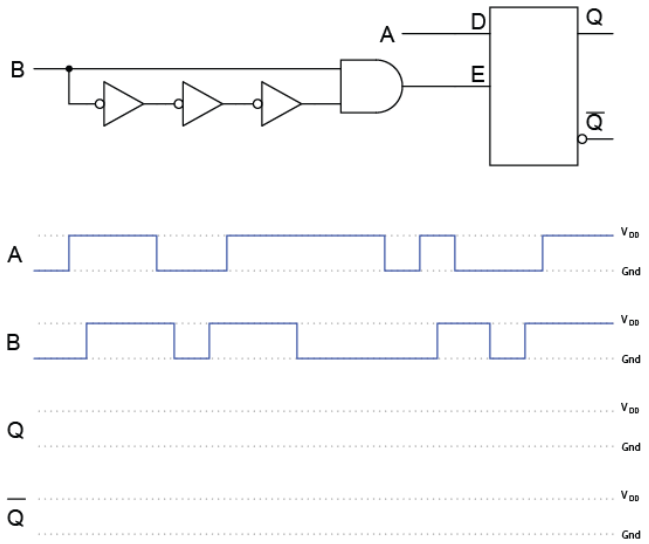

Figure 3.1 A D-type gated latch and the input

Question 3(b) **[5 marks]**

Determine the output states for the J-K flip-flop (as illustrated in Figure 3.2), given the pulse inputs shown at the bottom of Figure 3.2. Please sketch the output in your answer book.

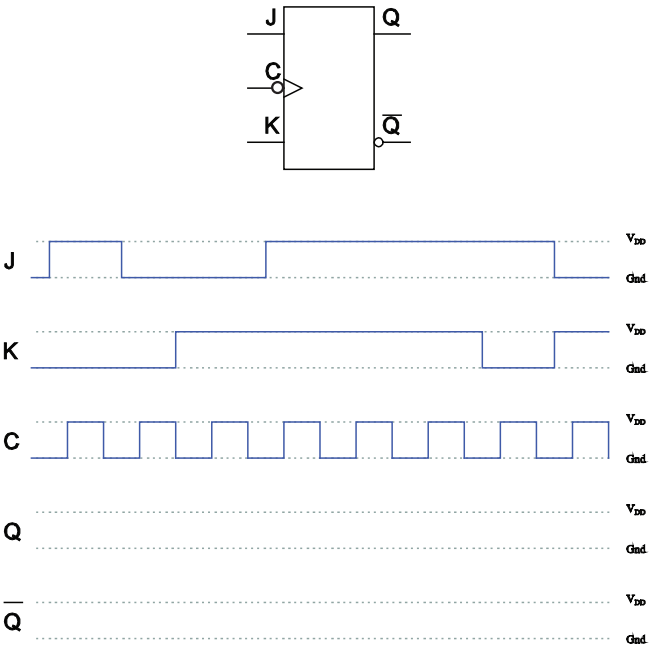

Figure 3.2 J-K flip-flop

Question 3(c) **[10 marks]**

Physical switches have to be carefully constructed to suit their environment and function. Discuss this statement, giving examples of different types of switches for different types of environments.

An S-R latch circuit can be used for switch *debouncing*. Explain what *bounce* refers to in mechanical switches and explain how the circuit described in Figure 3.3 eliminates it.

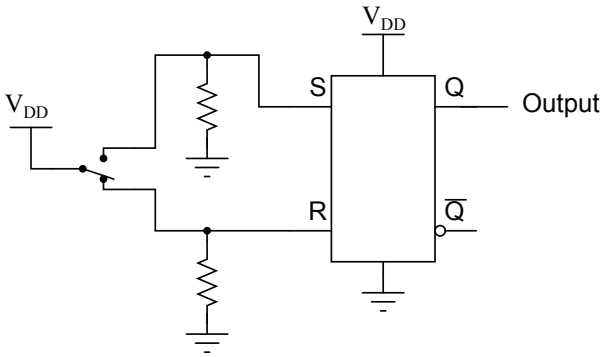

Figure 3.3 A circuit that can be used for switch debouncing.

[End of Question 3]

QUESTION 4 **[TOTAL MARKS: 25]**

Question 4(a) **[4 marks]**

Illustrate and explain the VOLTAGE/CURRENT characteristic of a PN Junction diode.

Question 4(b) **[9 Marks]**

A diode has the following characteristics:

V(V)	0	0.1	0.2	0.3	0.4	0.5	0.6
I(mA)	0	0.02	0.075	0.5	5.0	20.0	50.0

It is part of the following circuit as illustrated in Figure 4.1.

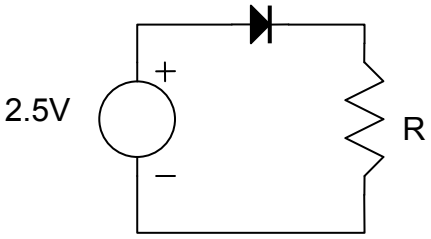

Figure 4.1 A Simple Diode Circuit

a) By graphical analysis, find the current through the circuit if R = 150Ω. Please request graph paper from the invigilator and secure it to your answer book.
b) What value of resistor will give a current of 20mA in the circuit and what will the voltage across the diode be?

Question 4(c) **[12 marks]**

Figure 4.2 illustrates some type of counter setup. The sequence that it generates is not a binary count. Determine what the counting sequence is and describe what modifications are required to the circuit to make it count in a proper binary sequence.

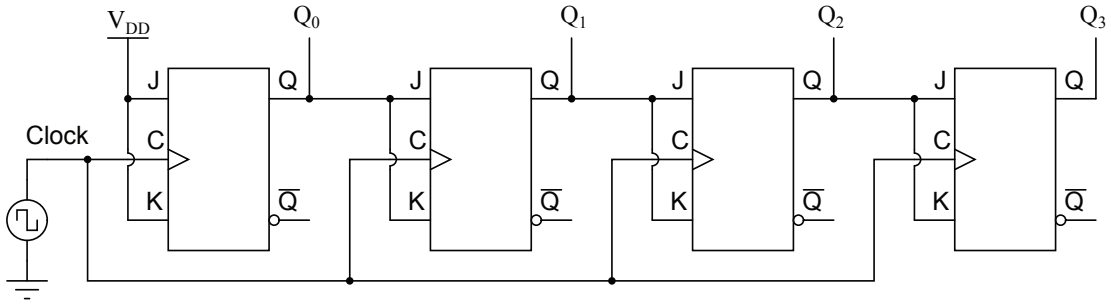

Figure 4.2 Some Type of Counter Setup

[End of Question 4]

QUESTION 5 **[TOTAL MARKS: 25]**

Question 5(a) **[8 marks]**

The circuit that is illustrated in Figure 5.1 has a transistor with h_{FE} =150.

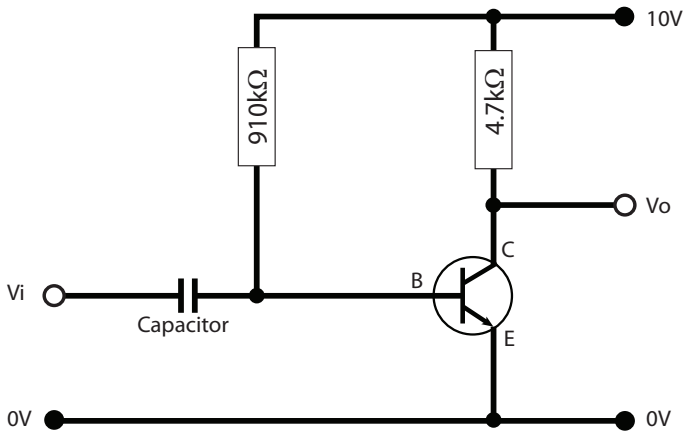

Figure 5.1 A basic transistor circuit

What do the letters CB and E represent in the figure? What type of transistor is illustrated and what does a h_{FE} =150 mean? What is the purpose of the capacitor? What is a suitable value to choose for V_{BE}?

Determine the quiescent collector current (*Ic*) and the quiescent output voltage (*Vo*) values.

Question 5(b) **[4 marks]**

Quantisation is used during the conversion of an analogue signal to its digital format. Explain what this means. A 10-bit ADC uses a reference voltage of 10V. Calculate the digital output value for an analogue input of 2.5V? What voltage will give a digital output of 678?

Question 5(c) **[13 marks]**

You are required to design a room temperature display system. You have been provided with an analogue temperature sensor that outputs a voltage between 0V and 5V where 0V represents -32 degrees Celsius and 5V represents 85 degrees Celsius. The temperature should be displayed on a 2-digit array of 7-segment displays.

Describe how you would design an Arduino microcontroller circuit to calculate and display the room temperature. Discuss your hardware setup, describing the input and output display circuits that you would design and how it would be connected to the Arduino. Also, give an outline of the code that you would write.

[End of Question 5]

[END OF EXAM]